Post-trial Motions Hearing

DEFENDANTS' MOTION FOR JMOL ON NON-INFRINGEMENT AND INVALIDITY (DKT. 578)

KAIST IP US OPPOSITION (DKT. 592)

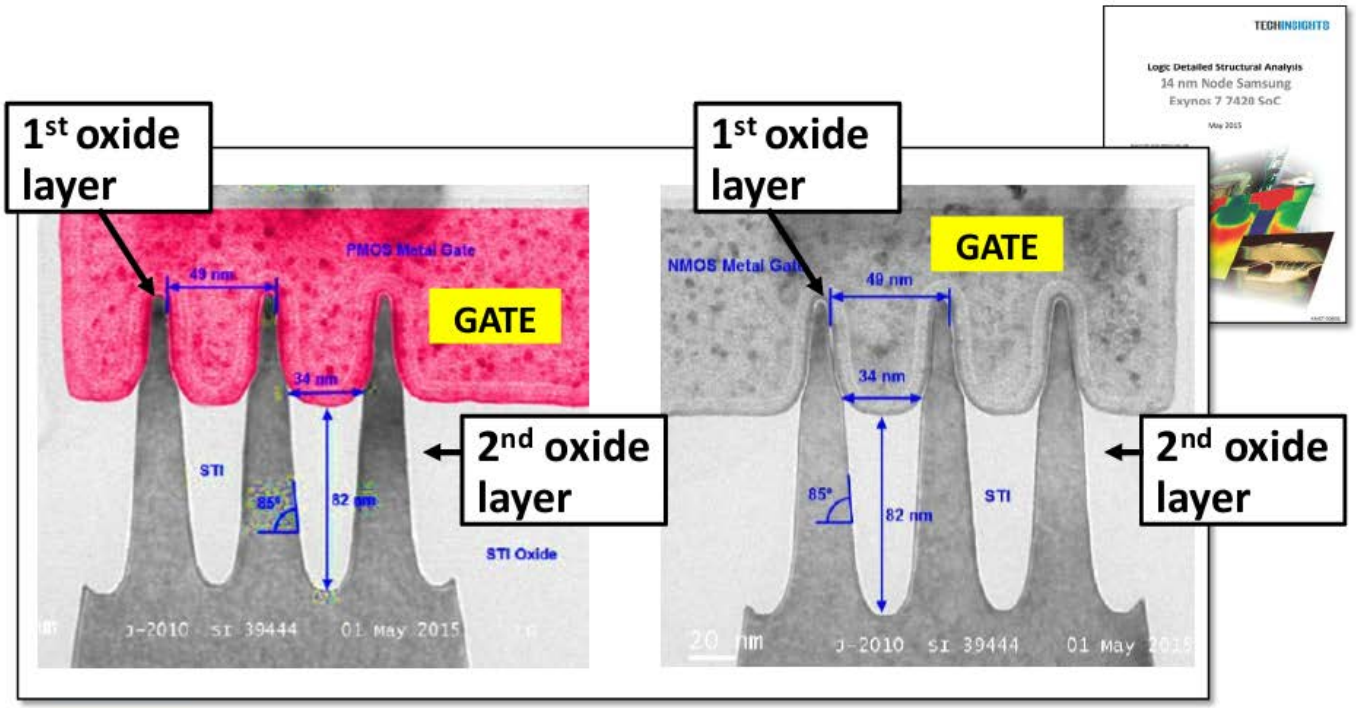
DEFENDANTS' REPLY (DKT. 602)

KAIST IP US SURREPLY (DKT. 618)

Gate Formed On Second Oxide Layer

Dr. Kuhn's Testimony to the Jury

TEMs Confirm



KAIST IP US LLC, v. SAMSUNG
PX0373
Case No. 2:16-CV-01314-JRG-RSP

Gate Annotated in Magenta

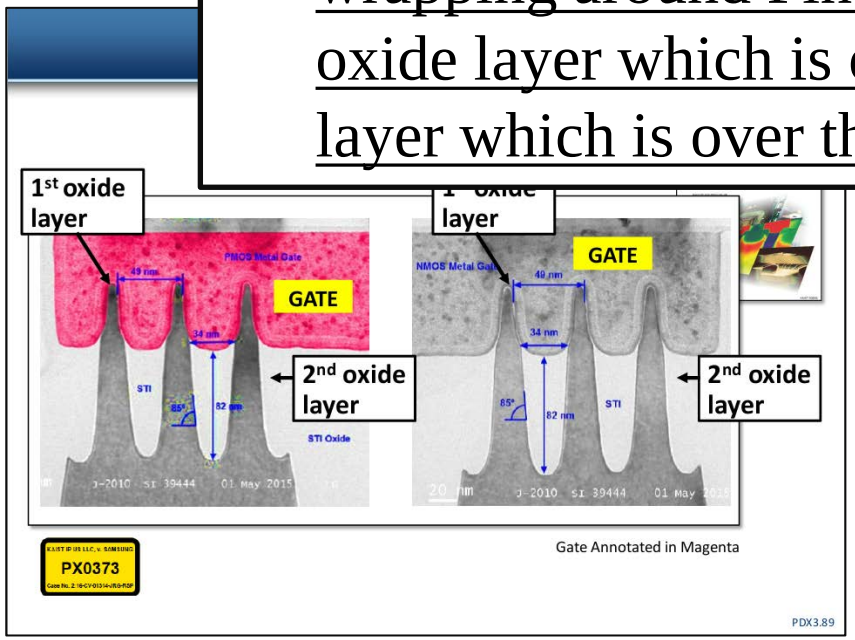
PDX3.89

Underlying images are in the record

Dr. Kuhn's Testimony to the Jury

Q. And what about TEM images, do they confirm this element, as well?

A. Yes. I'd like to point out Document PX-0373. And in PX-0373 I've indicated the gate in pink so it matches the model. And you can see the gate here, and it's wrapping around Fin active region, so it's on the first oxide layer which is on the top and the second oxide layer which is over there on the side.



Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 22:17-24 (emphasis added)

Dr. Subramanian Did Not Dispute Dr. Kuhn

Q. And there's nothing in your report that disputes that there's a gate which is formed on said first and second oxide layer, fair point?

A. With respect to the gate itself, that's true. I have not written --

Q. In your report, you don't discuss the limitation, a gate which is formed on said first and second oxide, fair point?

A. I don't remember specifically, but it certainly -- it sounds reasonable.

Q. You don't discuss it as a basis for non-infringement?

A. As – as an independent point, I think that's true.

Dkt. 496, **June 14, 2018 AM Trial Tr.** at 81:21-25 (cross) (emphasis added)

Dongwon Kim: SiO_2 and HfO Form "One Continuous Layer of Oxide"

Q. Now, Dr. Kim, the -- in the 14-nanometer devices, there is ***one continuous layer of oxide -- of gate oxide*** that wraps around all three sides of the Fin, correct?
A. Yes, that is correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 16:5-8 (cross)

Q. That ***gate oxide is a combination of silicon dioxide and Hafnium oxide***, correct?
A. That is correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 16:12-14 (cross)

Dongwon Kim Defines "One Oxide"

Q. And then there's a gate which is formed on the oxide that exists on all three sides, correct?

A. That is correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 16:5-11 (cross) (emphasis added)

Heedon Jeong: SiO_2 and HfO Form "One Continuous Oxide Layer"

QUESTION: And so just like in that figure, it's depicting ***one continuous – continuous oxide lay***er on all three sides of the Fin, correct?

ANSWER: Correct.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 52:9-12 (Heedon Jeong)

Dr. Kuhn: SiO_2 and HfO Form "One Layer"

Q. Now, what is this gate oxide layer in the accused devices made up of?

A. The gate oxide layer has two components. There's a component called Hafnium oxide, which is a dark color in these images. And there's a component called silicon oxide or silicon dioxide which is the light layer in the images.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 11:19-24 (Dr. Kuhn) (emphasis added)

Q. Do these components, ***the Hafnium oxide and the silicon dioxide, do these components operate as one layer***?

A. Yes, sir.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 12:9-11 (Dr. Kuhn)

Dr. Subramanian: SiO_2 and HfO Form "One Gate Oxide"

Q. After refreshing your recollection, you would agree that the accused devices have one gate oxide which -- which wraps around the surface?

A. Yes.

Q. And that one gate oxide is Hafnium oxide and silicon dioxide, fair?

A. Yes, it has both of those layers in there.

Q. Sir, let me reask the question. There's one gate oxide?

A. Yes, sir.

Q. Made up of Hafnium oxide and silicon dioxide, yes or no?

A. Yes, sir.

Dkt. 496, **June 14, 2018 AM Trial Tr.** at 85:17-86:1 (Subramanian cross) (emphasis added)

Dr. Wallace: SiO2 and HfO "Work Together to Form the Gate Oxide"

Q. (By Mr. Sheasby) So the gate oxide in the accused devices is composed of silicon dioxide and Hafnium oxide, correct?

A. That's correct.

Q. And they work together to form the gate oxide, correct?

A. That's correct.

Q. And so there is this gate oxide layer and on top of it is formed a gate, correct?

A. That's correct.

Dkt. 494, **June 13, 2018 AM Trial Tr.** at 196:18-197:1 (Wallace cross) (emphasis added)

SiO2 and HfO Combinations Were Not New

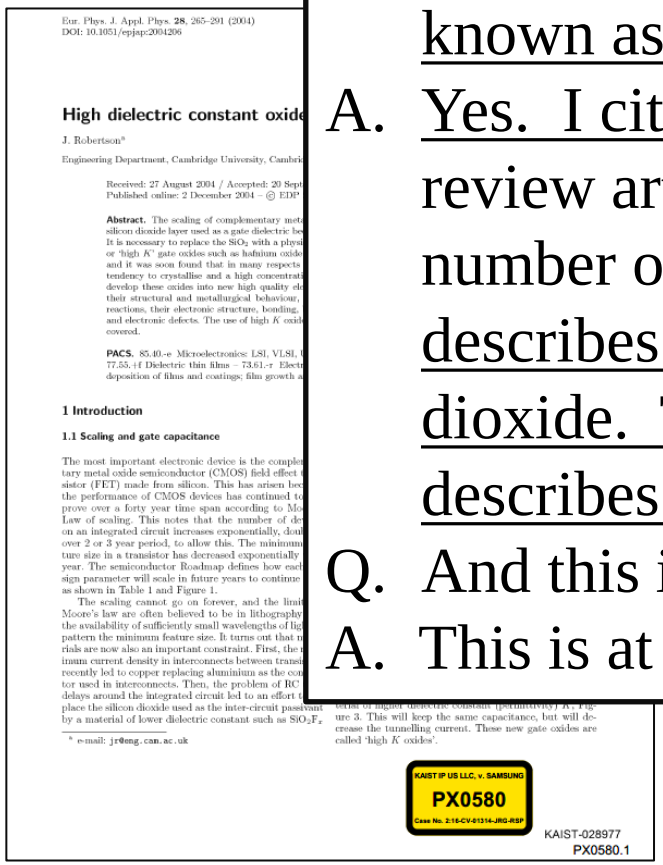
Dr. Kuhn's testimony to the jury:

Q. So was the idea of using these kinds of components, the Hafnium oxide and the silicon dioxide, was that known as a gate oxide layer?

A. Yes. I cite here an article from 2004. This is a review article. It's from Robertson. It cites a number of publications over prior decades, and it describes combinations of silicon dioxide, Hafnium dioxide. There is other High-k dioxides, and it also describes putting one on top of the other.

Q. And this is at PX-580?

A. This is at PX-580, correct.


Eur. Phys. J. Appl. Phys. **28**, 265–291 (2004)
DOI: 10.1051/epjap:2004206

High dielectric constant oxide

J. Robertson[a]

Engineering Department, Cambridge University, Cambri

Received: 27 August 2004 / Accepted: 20 Sept
Published online: 2 December 2004 – © EDP

Abstract. The scaling of complementary meta
silicon dioxide layer used as a gate dielectric be
It is necessary to replace the SiO_2 with a physi
or 'high K' gate oxides such as hafnium oxide
and it was soon found that in many respects
tendency to crystallise and a high concentrati
develop these oxides into new high quality el
their structural and metallurgical behaviour,
reactions, their electronic structure, bonding,
and electronic defects. The use of high K oxid
covered.

PACS. 85.40.-e Microelectronics: LSI, VLSI,
77.55.+f Dielectric thin films – 73.61.-r Electr
deposition of films and coatings; film growth a

1 Introduction

1.1 Scaling and gate capacitance

The most important electronic device is the comple
tary metal oxide semiconductor (CMOS) field effect
sistor (FET) made from silicon. This has arisen bec
the performance of CMOS devices has continued to
prove over a forty year time span according to Mo
Law of scaling. This notes that the number of de
on an integrated circuit increases exponentially, dou
over 2 or 3 year period, to allow this. The minimum
ture size in a transistor has decreased exponentially
year. The semiconductor Roadmap defines how each
sign parameter will scale in future years to continue
as shown in Table 1 and Figure 1.

The scaling cannot go on forever, and the limit
Moore's law are often believed to be in lithography
the availability of sufficiently small wavelengths of lig
pattern the minimum feature size. It turns out that n
risks are now also an important constraint. First, the
imum current density in interconnects between transi
recently led to copper replacing aluminium as the co
tor used in interconnects. Then, the problem of RC
delays around the integrated circuit led to an effort t
place the silicon dioxide used as the inter-circuit passivant
by a material of lower dielectric constant such as SiO_2F_x

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ure 3. This will keep the same capacitance, but will decrease the tunnelling current. These new gate oxides are called 'high K oxides'.

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KAIST-028977
PX0580.1

Dkt. 490, **June 12, 2018 AM Trial Tr. (sealed)** at 12:22-13:5 (emphasis added)

Prof. Lee: No Limits on Type of Gate Oxide in '055 Patent Specification

Q. Does your specification place any remnants [*sic*] on the composition of the gate oxide layer?

A. No, my patent specification allows for different materials to make up a gate oxide layer.

Dkt. 488, **June 11, 2018 AM Trial Tr.** at 86:17-20

Prof. Lee's Testimony Is Relevant

"[W]hen an inventor's understanding of a claim term is expressed in the prior art, it can be evidence of how those skilled in the art would have understood that term at the time of the invention."

-- ***ArcelorMittal France v. AK Steel Corp.,*** 700 F.3d 1314, 1322 (Fed. Cir. 2012)

Only Testimony in Record Regarding Plain Meaning

Dr. Kuhn: no limits on the composition of the oxide

Q. And the claims do not require any particular compensation [*sic*] to the gate oxide layer, do they?
A. No, sir.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 12:12-14

Only Testimony in Record Regarding Plain Meaning

Dr. Kuhn: claim language does not require the gate to be directly on the SiO_2 portion of the gate oxide

Q. And is there anything in the claims that require the gate to be directly on the SIO2 layer?
A. No, sir, there's nothing in the claims that says that the gate is directly on an SIO2 layer.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 23:2-5 (emphasis added)

Defendants Never Sought Narrowing Formed "Directly" Limitation

"Litigants waive their right to present new claim construction disputes if they are raised for the first time after trial."

-- ***Cordis Corp. v. Boston Sci. Corp.***, 561 F.3d 1319, 1331 (Fed. Cir. 2009) (citations, quotations omitted)

Defendants Never Sought Narrowing Formed "Directly" Limitation

Allowing the Defendant to make the intervening layer argument in opening: "Those are the ones you'll recall that have to do with the issue of formed on . . . and I've heard the arguments about whether or not this raises an issue of claim construction that requires a precise construction or guidance from the Court . . . ***do not find that argument as to the plain and ordinary meaning of the claim language itself as compared to the accused products is improper***"

Charging Conference: MR. CHOUNG: Your Honor, then from Plaintiffs in that regard, we'd like to renew our objections to the ruling on the claim construction for "directly formed on" to preserve the record.

6/11/18 AM at 139:24-140:
6/15/18 AM at 22:4-9

Defendants Never Sought Narrowing Formed "Directly" Limitation

"[I]f Lawson desired such a narrow definition, it could (and should) have sought a construction to that effect. In the absence of such a construction, however, the jury was free to rely on the plain and ordinary meaning of the term . . . ."

-- ***ePlus, Inc. v. Lawson Software,*** 700 F.3d 509, 520 (Fed. Cir. 2012)

Defendants' Formed "Directly" Construction Contradicts the Claim Language

"In the parlance of patent law, the transition 'comprising' creates a presumption that the recited elements are only a part of the device, that the claim does not exclude additional, unrecited elements."

-- ***Crystal Semiconductor Corp. v TriTech Microelectronics Intern. Inc.,*** 246 F.3d 1336, 1348 (Fed. Cir. 2001) (emphasis added)

Defendants' Formed "Directly" Construction Contradicts the Claim Language

Dr. Subramanian agreed with the definition of "comprising":

Q. Now, comprising means includes but not limited to; is that fair?

A. Yes, sir.

Q. Comprising allows you – comprising does not exclude additional features; is that fair?

A. That's true.

Q. And so when the jury considers infringement in this case and it looks at that work 'comprising,' you would agree that it should keep in mind that the claim doesn't exclude additional features?

A. In general, yes.

Dkt. 496, **June 14, 2018 AM Trial Tr.** at 80:8-15 (cross) (emphasis added)

Jury Instructed On DOE

"In order to prove direct infringement of a patent claim, the Plaintiff, KAIST, must show by a preponderance of the evidence that the accused product includes each and every element, requirement, or limitation of the claim either literally or under the Doctrine of Equivalents."

Dkt. 498, **June 15, 2018 Trial Tr.** at 46:5-9 (the Court) (emphasis added)

No Requirement that Expert Sponsor Formal DOE Opinion for Jury to Find Infringement by DOE

"West Bend argues that Presto did not provide sufficiently explicit witness testimony . . . ."

"[P]roof of equivalency is not a matter of formula, but of evidence appropriate to the case . . . . [N]o specific formulation of evidence and argument is required."

-- ***Nat. Presto Indus., Inc. v. West Bend Co.,*** 76 F.3d 1185, 1191 (Fed. Cir. 1996) (emphasis added)

SiO_2 and HfO "Operate as One Layer"

Dr. Kuhn:

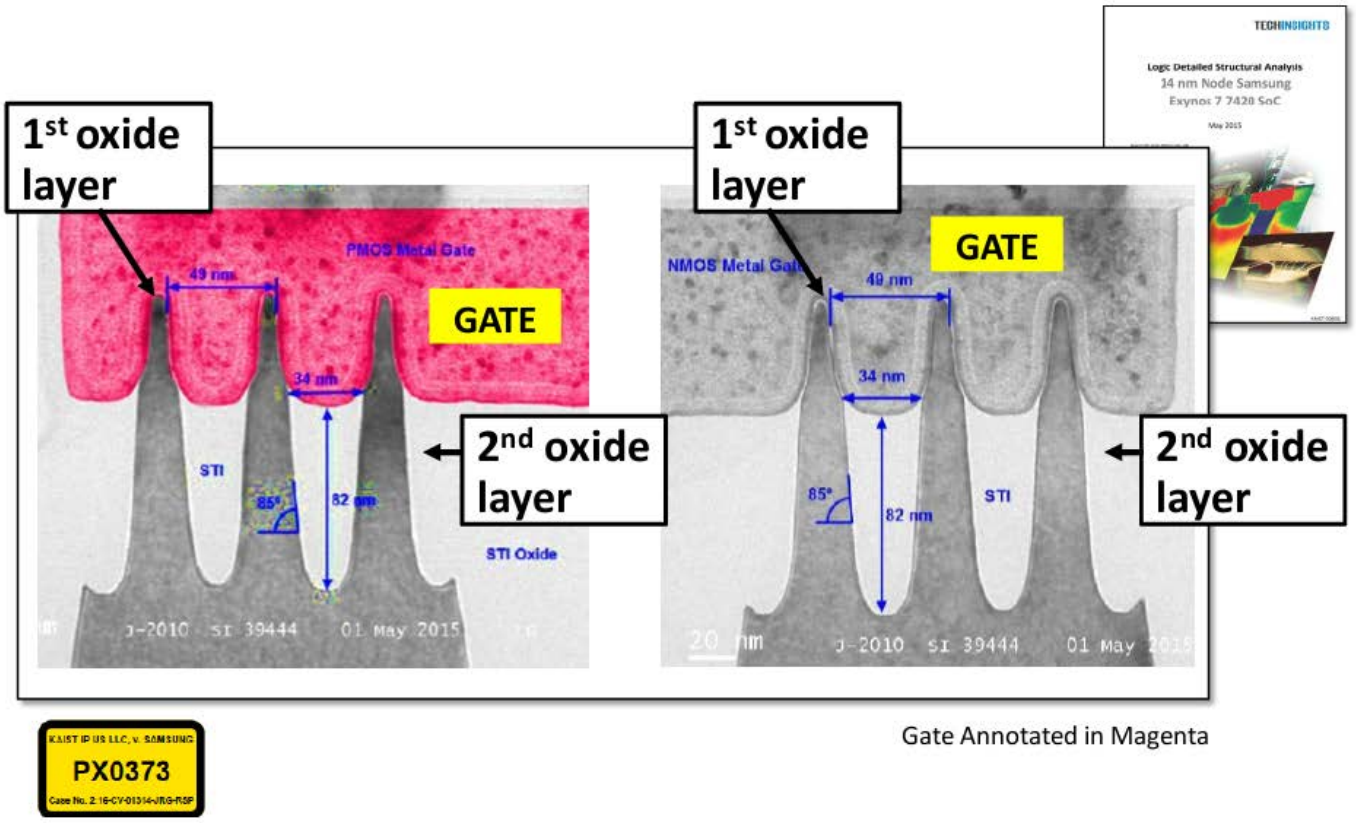
Q. Do these components, the Hafnium oxide and the silicon dioxide, do these components operate as one layer?
A. Yes, sir.

Dkt. 490, **June 12, 2018 AM Trial Tr. (sealed)** at 12:9-11

Gate Oxide Formed On First Oxide Layer

Dr. Kuhn's Demonstrative to the Jury

TEMs Confirm



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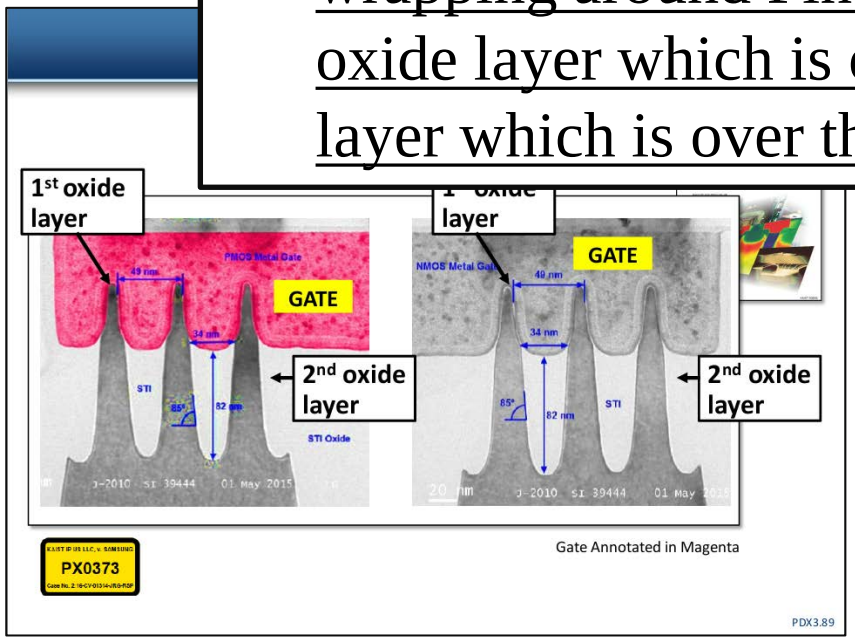


Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 22:17-24 (emphasis added)

SiO2 and HfO "Operate As One Layer"

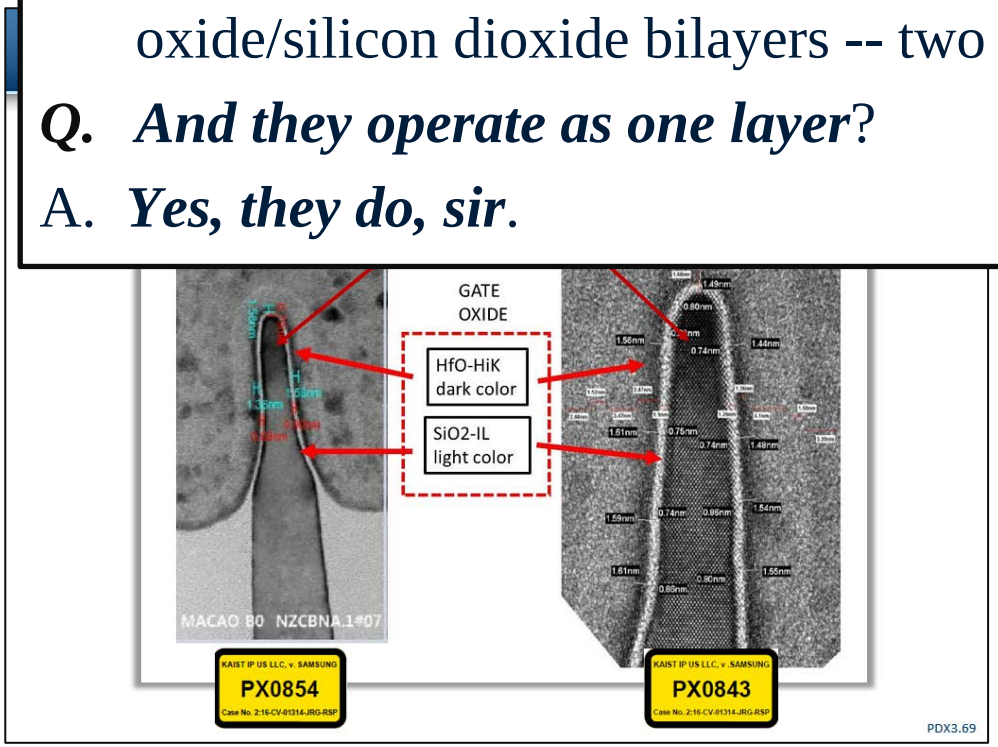
Dr. Kuhn's testimony to the jury:

Q. And do the Defendants' accused devices meet this limitation?

A. Yes, they do. I show here on the left Samsung document PX-0854, and on the right GlobalFoundries's document PX-0843. And I show that there is a first oxide on the top. And it is, again, one of these Hafnium oxide/silicon dioxide bilayers -- two oxides -- both are required.

Q. ***And they operate as one layer***?

A. ***Yes, they do, sir***.



Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 15:3-9

Dongwon Kim Admits That there is One Oxide: "the Oxide"

Q. Now, Dr. Kim, the -- in the 14-nanometer devices, there is one continuous layer of oxide -- of gate oxide that wraps around all three sides of the Fin, correct?

A. Yes, that is correct.

Q. And there there's a gate which is formed on the oxide that exists on all three sides, correct?

A. That is correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 16:5-11 (Dongwon Kim cross) (emphasis added)

Dongwon Kim: SiO_2 and HfO Form "One Continuous Layer of Oxide"

"One continuous layer of oxide -- of gate oxide"

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Dkt. 494, **June 13, 2018 PM Trial Tr.** at 16:5-8 (cross)

"gate oxide is a combination of silicon dioxide and hafnium oxide"

Q. That gate oxide is a combination of silicon dioxide and Hafnium oxide, correct?
A. That is correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 16:12-14 (cross)

Heedon Jeong: SiO_2 and HfO Form "One Continuous Oxide Layer"

QUESTION: And so just like in that figure, it's depicting one continuous – continuous oxide layer on all three sides of the Fin, correct?

ANSWER: Correct.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 52:9-12 (Heedon Jeong)

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Q. Now, what is this gate oxide layer in the accused devices made up of?
A. The gate oxide layer has two components. There's a component called Hafnium oxide, which is a dark color in these images. And there's a component called silicon oxide or silicon dioxide which is the light layer in the images.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 11:19-24 (Dr. Kuhn) (emphasis added)

Q. Do these components, ***the Hafnium oxide and the silicon dioxide, do these components operate as one layer***?
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Q. After refreshing your recollection, you would agree that the accused devices have one gate oxide which -- which wraps around the surface?

A. Yes.

Q. And that one gate oxide is Hafnium oxide and silicon dioxide, fair?

A. Yes, it has both of those layers in there.

Q. Sir, let me reask the question. There's one gate oxide?

A. Yes, sir.

Q. Made up of Hafnium oxide and silicon dioxide, yes or no?

A. Yes, sir.

Dkt. 496, **June 14, 2018 AM Trial Tr.** at 85:17-86:1 (Subramanian cross) (emphasis added)

Dr. Wallace: SiO_2 and HfO "Work Together to Form the Gate Oxide"

Q. (By Mr. Sheasby) So the gate oxide in the accused devices is composed of silicon dioxide and Hafnium oxide, correct?

A. That's correct.

Q. And they work together to form the gate oxide, correct?

A. That's correct.

Q. And so there is this gate oxide layer and on top of it is formed a gate, correct?

A. That's correct.

Q. And that gate oxide layer is formed on the Fin, correct?

A. That's correct.

Dkt. 494, **June 13, 2018 AM Trial Tr.** at 196:18-197:3 (Wallace cross) (emphasis added)

Upper Surface with Thickness Greater or Equal to Sidewalls

Claim Element Refers to Surfaces, Not Points

"a gate oxide layer which is formed on both **side-walls of the Fin active region protruded** from said second oxide layer"

"a first oxide layer which is formed on the **upper surface** of said Fin active region with a **thickness greater or equal to that of the gate oxide**"

Heedon Jeong Admitted Element Met

QUESTION: The oxide below the gate on ***all three sides of the Fin in Samsung's 40 – 14-nanometer process is generally equivalent in thickness***, correct?

ANSWER: ***They are equivalent***.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 47:16-20

QUESTION: Would you explain whether there are ***any differences between the gate oxide layer that resides along the sides walls and along top of the Fin***?

ANSWER: There is ***no difference on the gate oxide on the sides and the gate oxide on the top***.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 49:20-24

Heedon Jeong's Discussion Of Process Is Separate

ANSWER: On both sides and on top, and all of this is carried out as one process with the same thickness.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 49:13-14

Dr. Kuhn Concluded Element Met

A. I now want to talk about the thickness being greater or equal to that of the gate oxide. ***And in Samsung's case the thickness will be equal. And if it's equal, we will have gate control from both the top and the sides of the Fin***.

Q. So is this limitation met in the accused devices?

A. Yes.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 15:18-23

Samsung's Internal Documents Show Equal Thickness

Dr. Kuhn's testimony to jury:

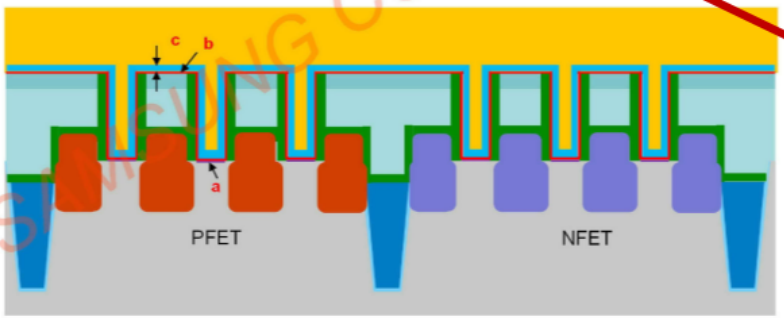
Defendants' Design Specifications Show Equal Thickness

SAMSUNG

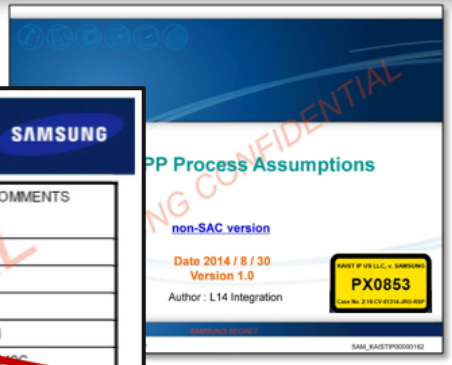
Structure Assumptions – RMG

SAMSUNG

PROCESS	THIN FILM / FEATURE	PARAMETER NAME	VALUE (nm)	TOL. (nm)	MEASUREMENT STRUCTURE	DESCRIPTION / COMMENTS
IL	IL THK (a)		1			
HK Deposition	HK THK (b)		1.5			
HK PN / PNA						
TiN Deposition	TiN THK (c)		5			ALD TiN
BARC Coating						Low Temp, 240C



System LSI Business - 76/96 - SAMSUNG SECRET 140830_TDC1_14LPP-FEOL-PA_Rev000



IL THK (a)
= SiO2 Oxide thickness for S/G transistors

HK THK (b)
= HfO thickness for all transistors

PDX3.76

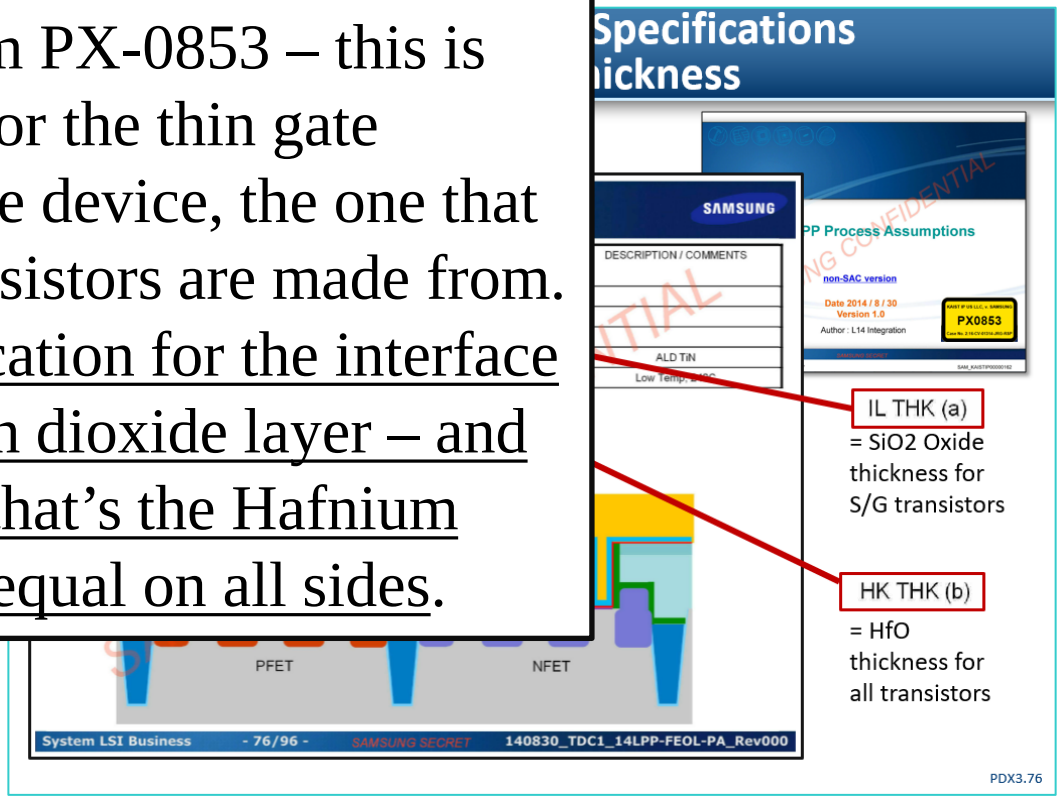
Samsung's Internal Documents Show Equal Thickness

Dr. Kuhn's testimony to the jury:

Q. And what else to the Defendants' internal documents show about this feature?

A. I also show, again, from PX-0853 – this is now the specification for the thin gate device, the performance device, the one that the majority of the transistors are made from. And <u>it shows a specification for the interface layer – that's the silicon dioxide layer – and for the High-k layer – that's the Hafnium layer – and it shows it equal on all sides</u>.

Dkt. 490, **June 12, 2018 AM Trial Tr. (Sealed)** at 16:16-24 (Dr. Kuhn) (emphasis added)



Dr. Kuhn Confirmed That Her Analysis Was Representative

Q. Now, what are the devices that you analyzed for infringement?

A. I analyzed transistors incorporating the Defendants' 14-nanometer bulk FinFET technology. There are two variants of the process the Defendants used. 14LPE, which is an early process, and 14LPP, which is their more mature process.

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 72:8-12

Q. And so is the analysis you're going to go through, is it ***representative of all the 14-nanometer LPE/LPP devices, chips,*** and products?

A. Yes, sir.

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 73:21-24

Dr. Kuhn's Methodology

Q. Now, did you also independently confirm these thicknesses with measurements?

A. Yes, sir, I did. I went to the TechInsights picture . . . . And I took their image and I added measurements of my own. These are these black squares here. ***And I did it in the same way I would have done if I'd been at Intel and asked to make a manual measurement. I then plotted these measurements over on the side, and I used warm colors for the upper surface, which would be the first oxide. And I used cool colors for the side surface, which would be the gate oxide***. And you see the same thing. Just like as in the Defendants' measurements, the top surface and the side surfaces are equal with manufacturing variation.

Dkt. 490, **June 12, 2018 AM sealed Trial Tr.** at 19:3-22

Dr. Kuhn's Methodology

Q. And the claims refer to the upper surface of the Fin, correct?

A. Yes, sir.

Q. All right. So ***in order to make the comparison between the side-walls and the upper surface, you need more than one point on the upper surface***?

A. Yes, sir.

Q. The claim does not say the tip of the Fin, does it?

A. No, it does not, sir.

Dkt. 489, **June 12, 2018 PM Trial Tr.** at 103:3-11

Dr. Kuhn's Methodology

Q. And in this case, how many -- how many sets of measurements, roughly, did you make in analyzing the Defendants' products?

A. I'm trying to remember, not even all of them are in my report because I have a summary table, but I ***remember doing at least six Fins for each of the situations that we had an analysis. So it was multiple samples because I wanted to make sure I had a large data set***.

Dkt. 489, **June 12, 2018 PM Trial Tr.** at 101:12-15

Dr. Kuhn's Conclusion

Q. And so when you take all the data that you measured, all the measurement data that you took, what were your average values?

A. My average values for the logic transistors, for all the data I had, ***was an upper surface measurement of 2.78 nanometers and a side-wall measurement of 2.65 nanometers***.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 171:16-21

Dr. Wallace Proposed Averaging to Determine Thickness

Q. . . . . You would agree that to measure a TEM image, ***it would be appropriate to average the thickness numbers at the top and sides of the Fin***, correct?

A. I would **--** ***I would agree that averaging would be appropriate***.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 185:1-5 (Wallace cross)

Dr. Kuhn's Conclusion

Dr. Kuhn's testimony to the jury:

Confirmed By Independent Measurements

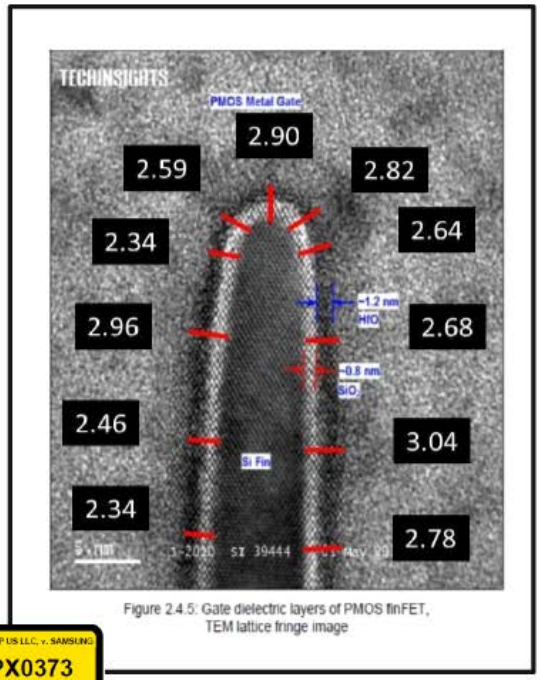
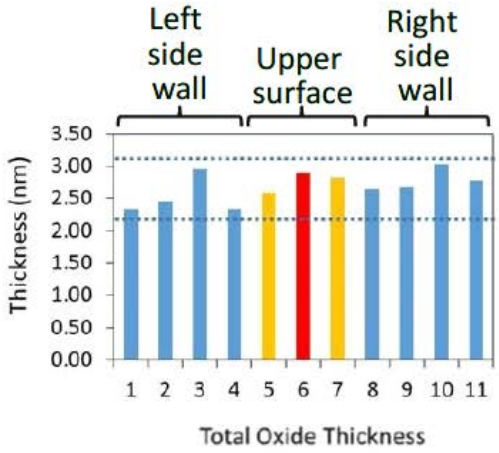


Figure 2.4.5: Gate dielectric layers of PMOS finFET, TEM lattice fringe image

KAIST IP US LLC, v. SAMSUNG
PX0373

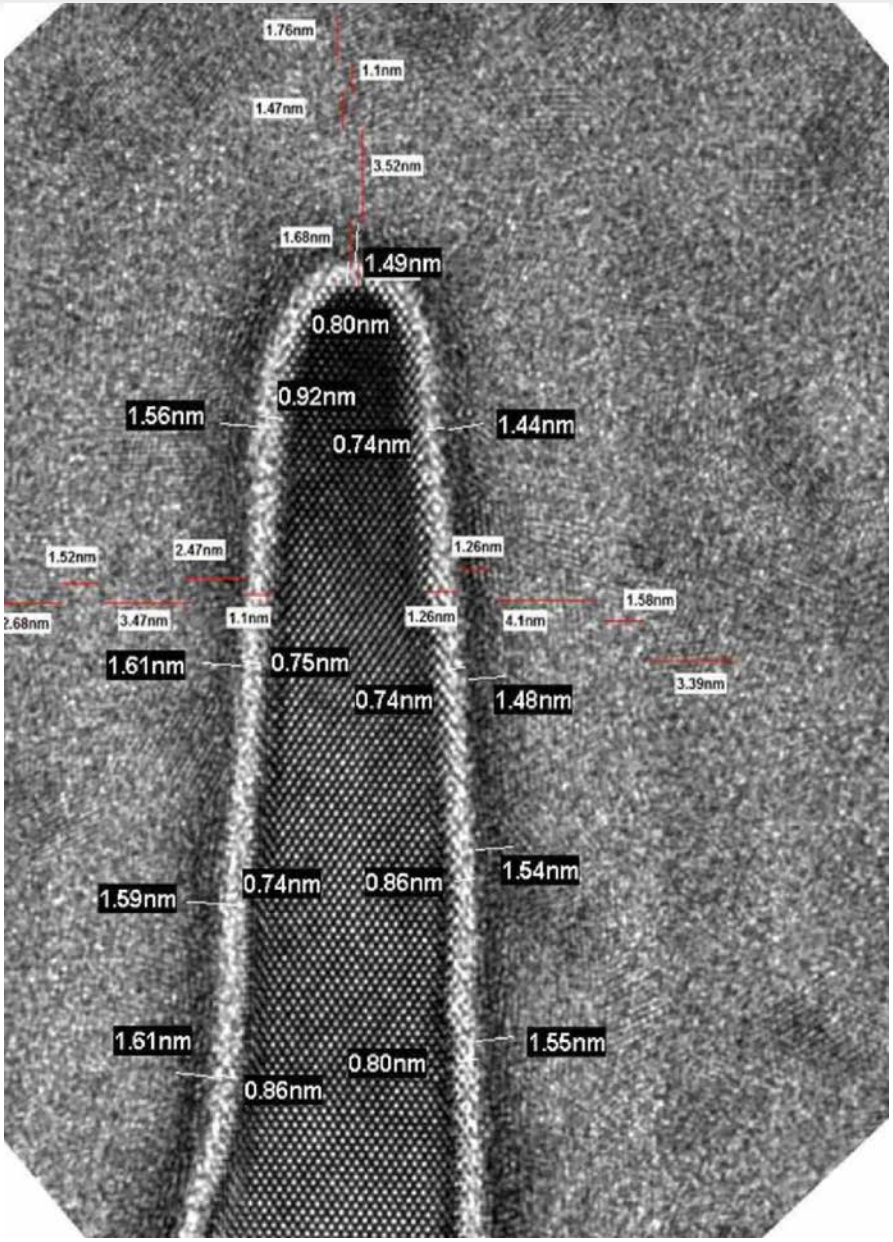


PMOS Transistor

Used same manual measurement protocol as Intel

PDX3.83

Dr. Kuhn's Conclusion



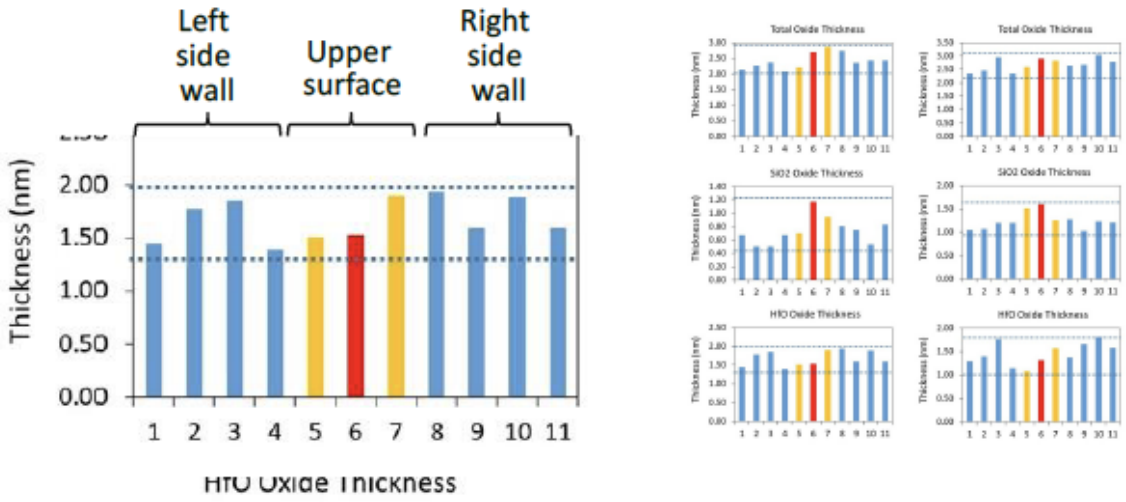
KAIST IP US LLC, v .SAMSUNG
PX0843
Case No. 2:16-CV-01314-JRG-RSP

Dr. Kuhn's Conclusion

Dr. Kuhn's testimony to the jury:

Average on Upper Surface and Sidewalls Is Equal

Examples of measurements made: logic device



All Measured Logic Transistors:

Measured **average**:
Upper surface: **2.78** nm
Sidewalls: **2.65** nm

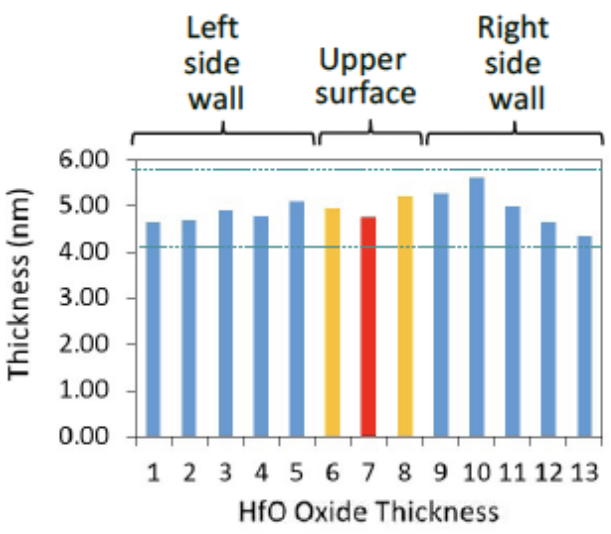
PDX3.93

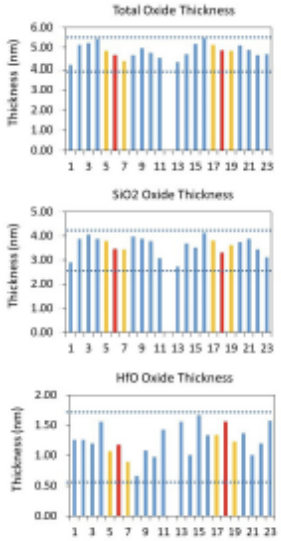
Dr. Kuhn's Conclusion

Dr. Kuhn's testimony to the jury:

Average on Upper Surface and Sidewalls Is Equal

Examples of measurements made: I/O device





All Measured I/O Transistors:

Measured **average**:

Upper surface: **5.13** nm

Sidewalls: **5.12** nm

PDX3.94

Dr. Kuhn's Conclusion

Q. And I noticed on the charts that you have here, for the upper surface you've actually got three data points?

A. Yes, sir, all ***my measurements that I made had three data points on the top***.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 171:22-25

Dr. Kuhn's Conclusion

Q. So then based on all the data that you've seen and measured and collected, what's your conclusion with respect to the thicknesses of the gate oxide in [*sic*] the first oxide?

A. All ***the data I've seen says the thicknesses on the top and the sides are equal***.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 172:16-20

Dr. Kuhn's Methodology

Q. But, do the Defendants consider this -- these thicknesses to be equal?

A. Yes. Dr. ***Samavedam says that the Hafnium dioxide layer, which is formed on all sides of the Fin, is intended to be of equal thickness and is, in fact, of equal thickness***.

Dkt. 490, **June 12, 2018 AM sealed Trial Tr.** at 18:16-19:22

Defendants Experts Provided No Alternative Data

Dr. Wallace:

Q. Now, you didn't measure the thickness in any of the images used in your report, correct?
A. Correct.

Dkt. 494, June 13, 2018 PM Trial Tr. at 185:6-7 (cross)

Dr. Subramanian:

Q. And you actually don't make any measurements whatsoever of any TEM, fair point?
A. Yes, sir.

Dkt. 496, June 14, 2018 PM Trial Tr. at 95:11-13 (cross)

Dr. Kuhn: Variance at Atomic Level Points On Surface

"If you look in the area here of the silicon dioxide component and the Hafnium component, you'll see the individual atomic layers there. This is actually a very nice film. It's very continuous and uniform around the Fin.

And it's an atomic layer film. ***If you think about it, it's kind of like they've wrapped marbles around the Fin at the atomic level***.

And as you can imagine, if ***you're wrapping marbles around the Fin, there's going to be some manufacturing variation***."

Dkt. 490, **June 12, 2018 AM Trial Tr. (sealed)** at 17:13-22

Dr. Samavedam: Layer Still Equal On Sidewalls And Upper Surface Despite Atomic Point Variance

Q. (By Mr. Sheasby) I'll represent to you that Dr. Kuhn prepared this demonstrative showing the thicknesses of the Hafnium oxide layer at different positions in the Fin. ***Would it surprise you that there are those types of variances in the Hafnium oxide thickness in the 14-nanometer FinFET devices***?

A. No.

Q. Despite those variances, ***the thickness of the High-k or Hafnium oxide layer that wraps around the Fin is equal, correct***?

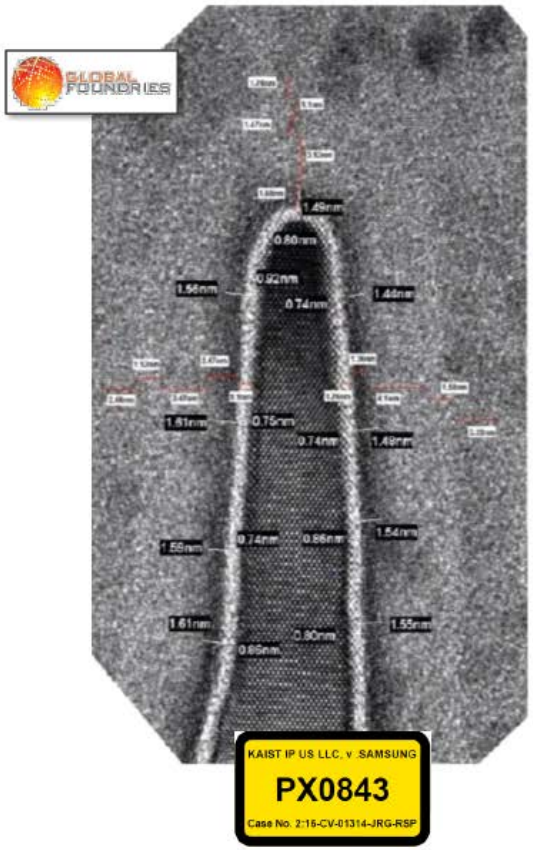
A. Yes.

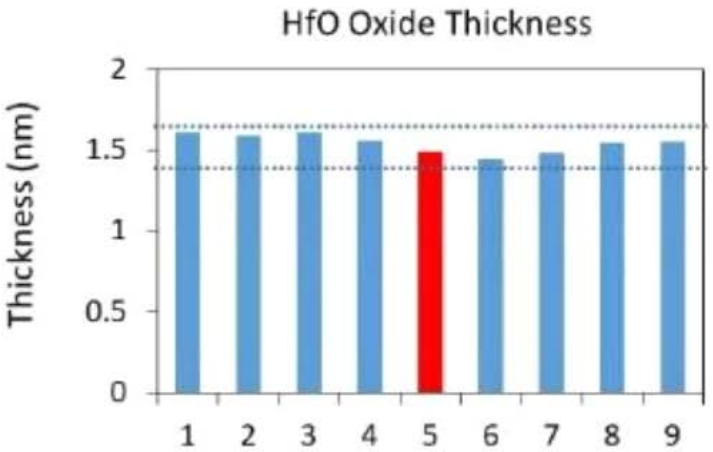
Dkt. 494, **June 13, 2018 PM Trial Tr.** at 112:16-19 (cross)

HfO Variance

Dr. Kuhn's testimony to the jury:

Equal Thickness In Real World





PDX3.80

Understanding of POSA Must Be Considered

"The meaning of patent terms depends on the usage of those terms in context by one of skill in the art at the time of application."

-- ***Middleton, Inc. v. 3M Co.***, 311 F.3d 1384, 1389 (Fed. Cir. 2002).

Dr. Subramanian: POSA Reading the Claim Understands Atomic Point Variance

Q. In other words, when a ***person of ordinary skill in the art is reading the '055 patent and reading the claim that says equal thickness on the upper surface and equal thickness on the side walls, that person is reading that patent with the understanding of manufacturing tolerances***, fair point?

A. Yes, sir.

Dkt. 494, **June 14, 2018 AM Trial Tr.** at 99:20-100:1 (cross)

Dr. Kuhn Performed Proper DOE Analysis

Q. So even with manufacturing variation then is the limitation met under the, for example, Doctrine of Equivalents?

A. Yes, it would be. And under the Doctrine of Equivalents, ***the differences in the oxide layer thicknesses are insubstantial***. I might point out that if they were insubstantial, Samsung would have problems with its devices. But they're insubstantial, they have substantially -- excuse me -- the same function, and preventing short circuiting between the Fin active region and the gate in substantially the same way by using a thin layer of insulating oxide material that does not conduct charge carriers to provide the same result in preventing the flow of charge carriers between the Fin active region and gate.

Dkt. 490, **June 12, 2018 AM Trial Tr. (sealed)** at 20:11-25

Defendants Admit Gate Function on All Three Sides

QUESTION: There's a gate oxide that's present on both sides of the Fin, correct?

ANSWER: Yes, gate oxide. And the gate wraps around the Fin, all three sides of the Fin.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 46:22-23 (Heedon Jeong)

Q. Now, you said something interesting to me. You called your device a tri-gate device. Do I have your testimony correct?
A. Yes.
Q. And what you referred to as a tri-gate device is describing a gate that surrounds all sides of the Fin, correct?
A. Yes.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 104:22-105:4 (Samavedam cross)

No Vitiation

- Defendants: Every point on the upper surface must be thicker than or equal to every point on both sidewalls

- Dr. Kuhn: average equal thickness between upper surface and sidewalls is equivalent

Fin Active Region Which is a Wall-Shape Single Crystalline Silicon

Heedon Jeong Admitted Element Present

QUESTION: Now, the ***Fin active region in the 14-nanometer devices is on the surface of the bulk silicon sub***strate, correct?

ANSWER: Yes.

QUESTION: ***It's a wall-shape single crystalline silicon***?

ANSWER: Yes, that's a single crystalline.

QUESTION: The answer to my question is yes, then?

ANSWER: ***Yes***.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 47:21-48:4

Dr. Wallace Admitted Distinct Side and Upper Surfaces

Q. And here, up here, that circle is the upper surface of the Fin, correct?
A. Correct.
Q. Upper surface is not one point, correct?
A. It's a region, that's correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 194:23-195:2 (cross)

Q. (So we agree that the Fins in this case have side-walls, correct?
A. Correct.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 195:15-17 (cross)

Dr. Kuhn Concluded Element Literally Present

Q. Now, what's the next element that you analyze?

A. The next element I analyze is a Fin active region, which is a wall-shape single crystal silicon on a surface of a bulk silicon substrate and connected to said bulk silicon substrate. And I broke it into three pieces. ***The first pieces is the Fin active region, which is a wall-shaped single crystal silicon***. And then the other two pieces are on the surface of the bulk silicon substrate and connected to the bulk silicon substrate.

Q. And do the Defendants' accused devices include this element?

A. Yes.

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 76:9-20

Dr. Kuhn Concluded That Samsung's Design is Fully Depleted

"And what I show here is PX-0852. This is an internal Samsung document. What you see in the document is the wall-shape Fin active region, as we've talked about with Professor Lee's testimony. That wall-shape Fin active region is what creates the fully depleted region that allows for the improved short channel effects."

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 77:2-8 (emphasis added)

Dr. Kuhn Concluded That Samsung's Design is Fully Depleted

A. This is this point of the wall-shaped Fin active region creating a fully depleted region in the device. Keep in mind in the '055 patent, ***the shape of the Fin active region, the wall-shape creates a fully depleted region, and that's important for producing the short channel effects***.''

June 14, 2018 PM Trial Tr. at 131:5-9

Dr. Kuhn Concluded That Samsung's Design is Fully Depleted

"Yes, there are. And I show here on the left Samsung's documents, PX-0863, and on the right, GlobalFoundries documents, PX-0208. And I'll orient the Fin for the jury. It's right straight at you. And you can see the wall-shape Fin active region there."

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 78:5-9 (emphasis added)

Dr. Kuhn Responded to "Parabola" Argument

A. I ***understand their argument is based on that the – that a wall would be flat on the top and sharp corners, not rounded***.

Q. Now, are rounded Fins still wall-shaped?

A. Yes, sir. And we can see this from Claim 15. Remember Claim 15 is a part of the patent claims. It includes the devices claimed in Claim 1, and that includes the Fin active region and wall-shape language. And it adds the comment: ***Wherein the top two corners of said Fin active region are chamfered. And so the Court has defined chamfered to be beveled or rounded. So that would be the top two corners of the Fin active region are beveled or rounded. So the patent itself contains language that has in it the idea of beveled or rounded Fins. So they're clearly part of what Professor Lee was thinking about when he used the term "wall-shape."***

Dkt. 490, **June 12, 2018 AM Trial Tr. (sealed)** at 5:11-6:3

Dr. Kuhn's DOE Analysis

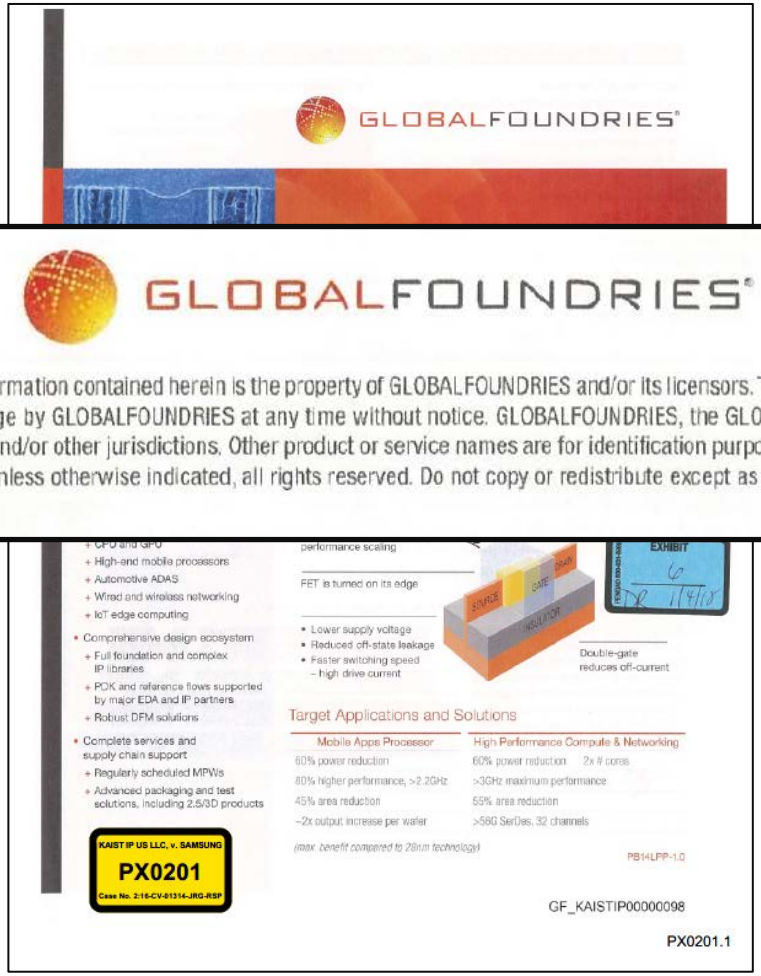
Q. Now, would this element also be met under the Doctrine of Equivalents?

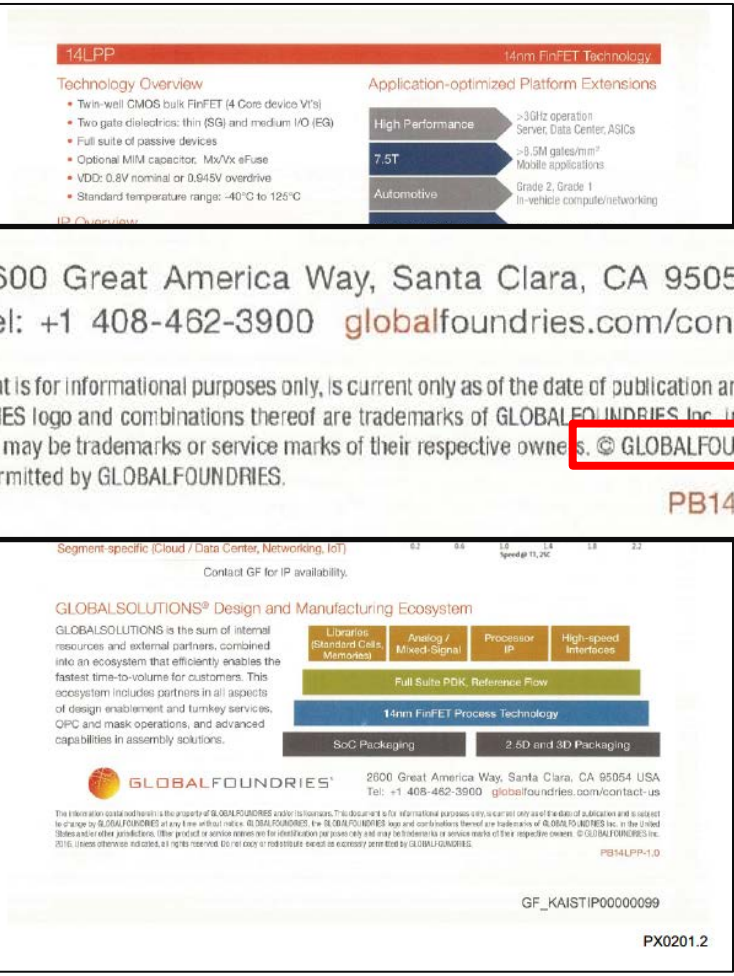
A. Yes, sir. And under the Doctrine of Equivalents, this element, the wall-shape Fin active region, would provide substantially the same function; that is, providing an increased channel area here along which the gate acts to control the flow of charge carriers. In substantially the same way, a tall narrow channel rising from the plane of the substrate to achieve the same results. And that, of course, is the improved on/off channel characteristics, the improved short channel effects over planar structures.

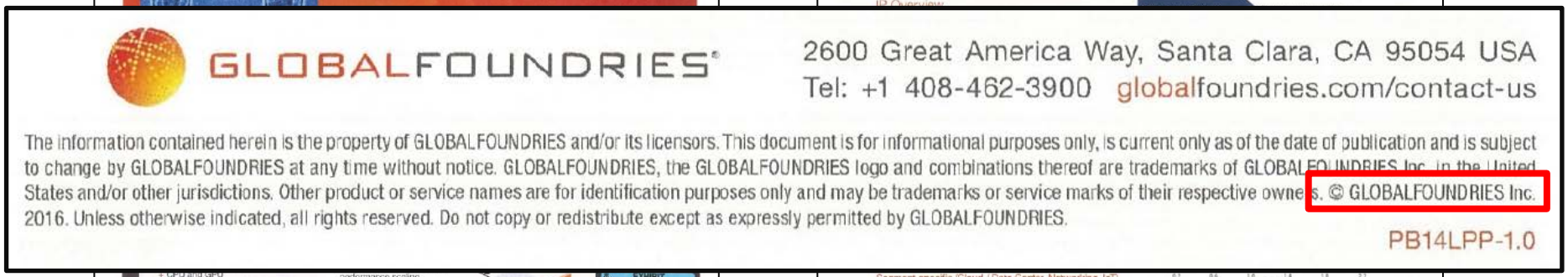
Dkt. 490, **June 12, 2018 AM Trial Tr. (sealed)** at 6:7-18

Substantial Evidence That GFI Infringed

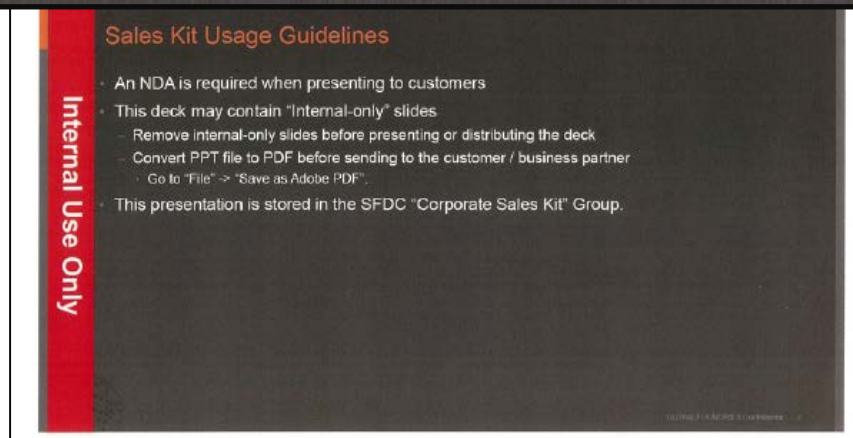
GFI Published GlobalFoundries' 14LPP Offer Sheet







GFI Published GlobalFoundries' 14LPP Sales Kit



RESTRICTED - ATTORNEYS' EYES ONLY GF_KAISTIP00000318

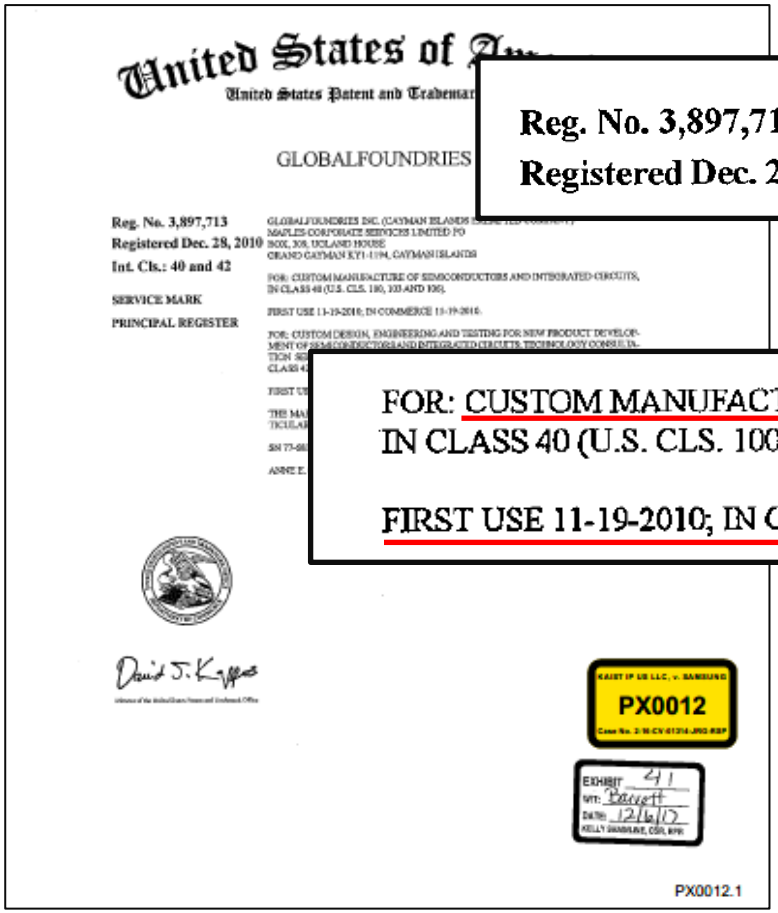
KAIST IP US LLC, v. SAMSUNG
PX0202
Case No. 2:16-CV-01314-JRG-RSP

PX0202.2

RESTRICTED - ATTORNEYS' EYES ONLY GF_KAISTIP00000399

PX0202.83

GFI Owns the GlobalFoundries Trademarks



United States of A...
United States Patent and Tradema...

GLOBALFOUNDRIES

Reg. No. 3,897,713
Registered Dec. 28, 2010
Int. Cls.: 40 and 42

SERVICE MARK
PRINCIPAL REGISTER

PX0012

EXHIBIT 41
DATE 12/6/17

PX0012.1

Reg. No. 3,897,713
Registered Dec. 28, 2010

GLOBALFOUNDRIES INC. (CAYMAN ISLANDS EXEMPTED COMPANY)
MAPLES CORPORATE SERVICES LIMITED PO
BOX, 309, UGLAND HOUSE
GRAND CAYMAN KY1-1194, CAYMAN ISLANDS

FOR: CUSTOM MANUFACTURE OF SEMICONDUCTORS AND INTEGRATED CIRCUITS, IN CLASS 40 (U.S. CLS. 100, 103 AND 106).

FIRST USE 11-19-2010; IN COMMERCE 11-19-2010.

GFI Declared that It Uses Trademarks in Commerce for Semiconductors and Integrated Circuits

United States of America
United States Patent and Trademark Office

Specimen File1
Specimen File2
Original PDF file:
SPN0-12226163-125910207_.s_40_and_42_design_solutions_advanced_technologies_09022010.PDF
Converted PDF file(s) (2 pages)
Specimen File1
Specimen File2

For International Class 042:

Declaration

Applicant requests registration of the above-identified trademark/service mark in the United States Patent and Trademark Office on the Principal Register established by the Act of July 5, 1946 (15 U.S.C. Section 1051 et seq., as amended). Applicant is the owner of the mark sought to be registered, and is using the mark in commerce on or in connection with the goods/services identified above, as evidenced by the attached specimen(s) showing the mark as used in commerce.

THE MARK CONSISTS OF STANDARD CHARACTERS WITHOUT CLAIM TO ANY PARTICULAR FONT, STYLE, SIZE, OR COLOR.

SN 77-661,676, FILED 3-2-2009.

ANNE E. GUSTASON, EXAMINING ATTORNEY

David J. Kappos

KAIST IP US LLC, v. SAMSUNG
PX0012
Case No. 2:16-CV-01314-JRG-RSP

EXHIBIT 41
WIT: Barrett
DATE: 12/6/17
KELLY SHAMBLIN, CSR, RPR

PX0012.1

SPN1-12226163-125910207_.Specimens_for_class_42_design_cadence_pdks_09022010.pdf
Converted PDF file(s) (5 pages)
Specimen File1
Specimen File2
Specimen File3
Specimen File4
Specimen File5
Original PDF file:
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Converted PDF file(s) (2 pages)
Specimen File1
Specimen File2

The applicant is not filing a Request to Divide with this Allegation of Use form.

A fee payment in the amount of $200 will be submitted with the form, representing payment for the allegation of use for 2 classes.

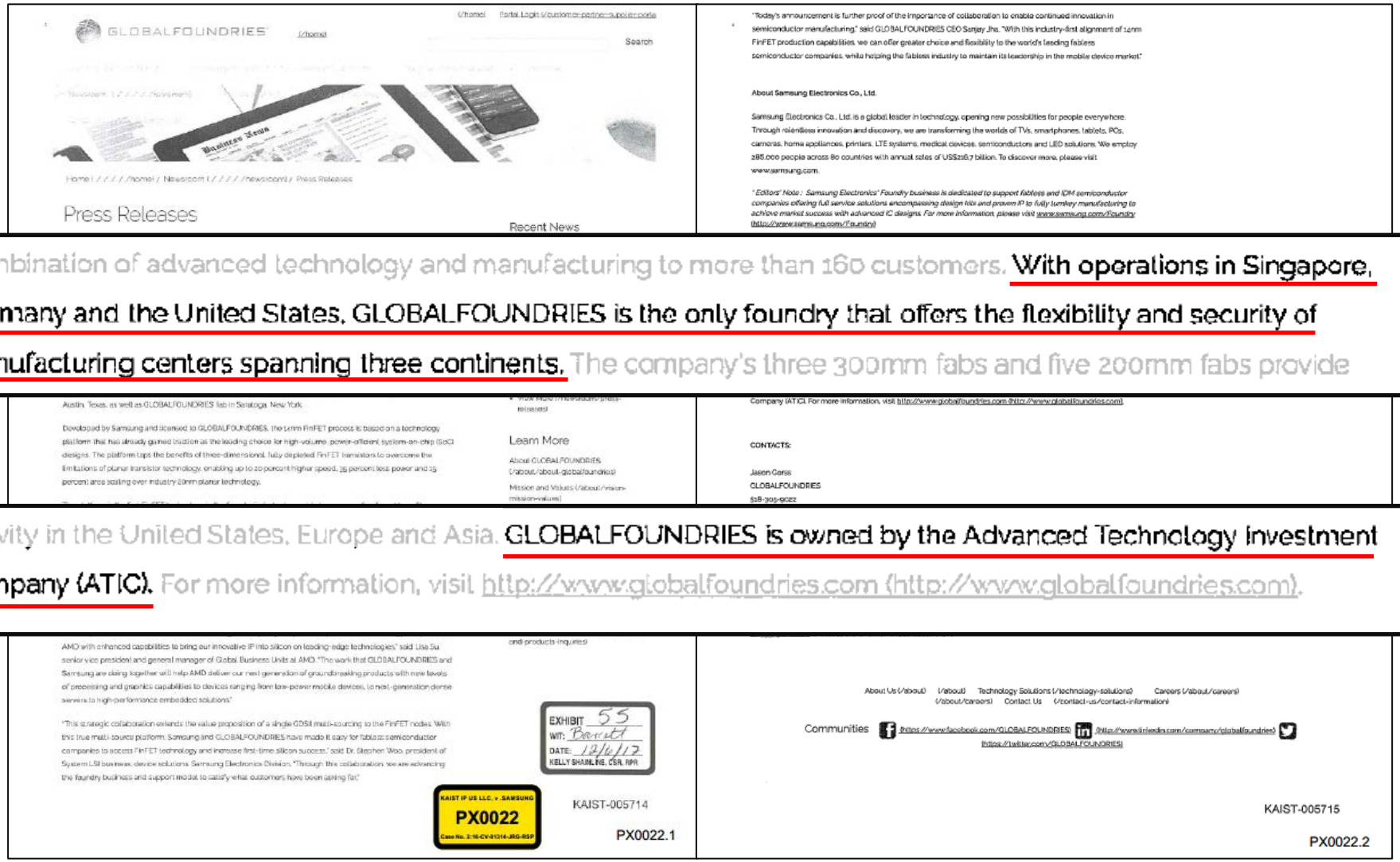
Declaration

Applicant requests registration of the above-identified trademark/service mark in the United States Patent and Trademark Office on the Principal Register established by the Act of July 5, 1946 (15 U.S.C. Section 1051 et seq., as amended). Applicant is the owner of the mark sought to be registered, and is using the mark in commerce on or in connection with the goods/services identified above, as evidenced by the attached specimen(s) showing the mark as used in commerce.

The undersigned, being hereby warned that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. Section 1001, and that such willful false statements may jeopardize the validity of the form or any resulting registration, declares that he/she is properly authorized to execute this form on behalf of the applicant; he/she believes the applicant to be the owner of the

PX0012.6

Joint Samsung/GloFo Press Release Identifies GFI



GLOBALFOUNDRIES

Press Releases

Recent News

"Today's announcement is further proof of the importance of collaboration to enable continued innovation in semiconductor manufacturing," said GLOBALFOUNDRIES CEO Sanjay Jha. "With this industry-first alignment of 14nm FinFET production capabilities, we can offer greater choice and flexibility to the world's leading fabless semiconductor companies, while helping the fabless industry to maintain its leadership in the mobile device market."

About Samsung Electronics Co., Ltd.

Samsung Electronics Co., Ltd. is a global leader in technology, opening new possibilities for people everywhere. Through relentless innovation and discovery, we are transforming the worlds of TVs, smartphones, tablets, PCs, cameras, home appliances, printers, LTE systems, medical devices, semiconductors and LED solutions. We employ 286,000 people across 80 countries with annual sales of US$216.7 billion. To discover more, please visit www.samsung.com.

** Editors' Note: Samsung Electronics' Foundry business is dedicated to support fabless and IDM semiconductor companies offering full service solutions encompassing design kits and proven IP to fully turnkey manufacturing to achieve market success with advanced IC designs. For more information, please visit www.samsung.com/Foundry (http://www.samsung.com/Foundry)*

combination of advanced technology and manufacturing to more than 160 customers. With operations in Singapore, Germany and the United States, GLOBALFOUNDRIES is the only foundry that offers the flexibility and security of manufacturing centers spanning three continents. The company's three 300mm fabs and five 200mm fabs provide

Austin, Texas, as well as GLOBALFOUNDRIES' fab in Saratoga, New York.

Developed by Samsung and licensed to GLOBALFOUNDRIES, the 14nm FinFET process is based on a technology platform that has already gained traction as the leading choice for high-volume, power-efficient system-on-chip (SoC) designs. The platform taps the benefits of three-dimensional, fully depleted FinFET transistors to overcome the limitations of planar transistor technology, enabling up to 20 percent higher speed, 35 percent less power and 15 percent area scaling over industry 20nm planar technology.

Learn More

About GLOBALFOUNDRIES (/about/about-globalfoundries)

Mission and Values (/about/vision-mission-values)

Company (ATIC). For more information, visit http://www.globalfoundries.com (http://www.globalfoundries.com).

CONTACTS:

Jason Gorss
GLOBALFOUNDRIES
518-305-9022

activity in the United States, Europe and Asia. GLOBALFOUNDRIES is owned by the Advanced Technology Investment Company (ATIC). For more information, visit http://www.globalfoundries.com (http://www.globalfoundries.com).

AMD with enhanced capabilities to bring our innovative IP into silicon on leading-edge technologies," said Lisa Su, senior vice president and general manager of Global Business Units at AMD. "The work that GLOBALFOUNDRIES and Samsung are doing together will help AMD deliver our next generation of groundbreaking products with new levels of processing and graphics capabilities to devices ranging from low-power mobile devices, to next-generation dense servers to high-performance embedded solutions."

"This strategic collaboration extends the value proposition of a single GDSII multi-sourcing to the FinFET nodes. With this true multi-source platform, Samsung and GLOBALFOUNDRIES have made it easy for fabless semiconductor companies to access FinFET technology and increase first-time silicon success," said Dr. Stephen Woo, president of System LSI business, device solutions, Samsung Electronics Division. "Through this collaboration, we are advancing the foundry business and support model to satisfy what customers have been asking for."

EXHIBIT 55
WIT: Barnett
DATE: 12/6/17
KELLY SHAINLINE, CSR, RPR

KAIST IP US LLC, v. SAMSUNG
PX0022
Case No. 2:16-CV-01314-JRG-RSP

KAIST-005714

PX0022.1

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KAIST-005715

PX0022.2

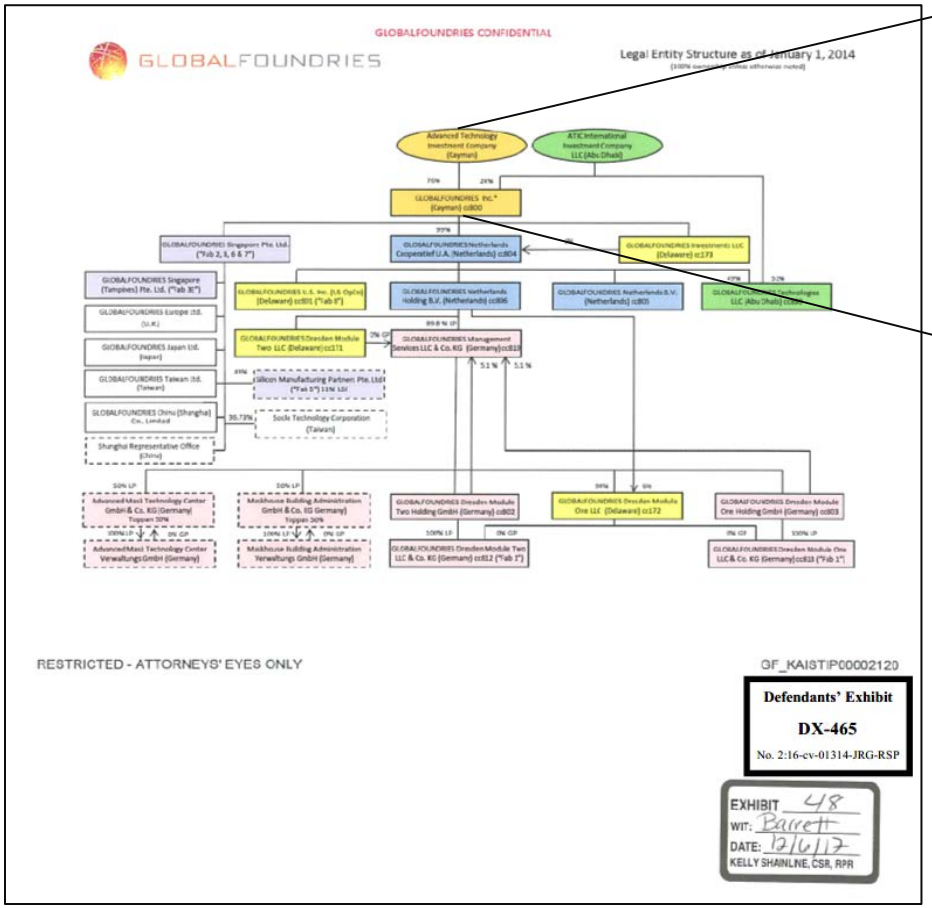
Joint Samsung/GloFo Press Release Identifies GFI

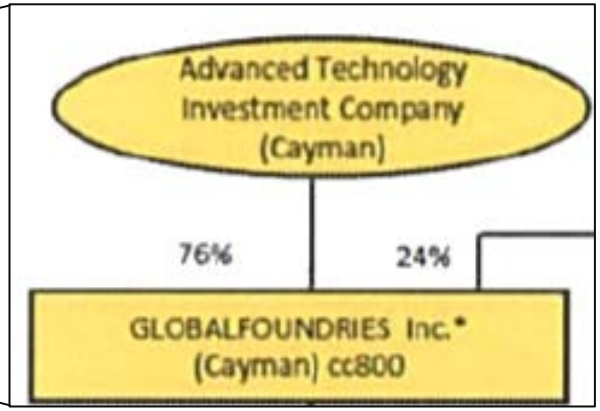
QUESTION: So this is Exhibit 55.
ANSWER: Uh-huh.
QUESTION: I think you'll recognize this as a press release.
ANSWER: Uh-huh.
QUESTION: And I want to call your attention to the second page. About midway, there's a section called about GlobalFoundries. Do you see that?
ANSWER: Yes.
QUESTION: Oh, and just to make sure that there's no confusion, if you look at the third page --
ANSWER: Uh-huh.
QUESTION: -- at the very top, it says: GlobalFoundries, Inc., is the owner in the United States. Do you see that phrase?
ANSWER: Yeah.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 77:10-25 (William Barrett)

Joint Samsung/GloFo Press Release Identifies GFI

GFI is the only entity owned by ATIC:





Case Law Does Not Require Pricing

"Were the lack of definitive pricing or the prospect of an immediate sale dispositive, sellers of products that by their nature defy such pricing and are incapable of being purchased in a prototypical way . . . would be out of reach for the purpose of specific personal jurisdiction, free to peddle their allegedly infringing wares in any forum without having made an 'offer to sell.' As the Federal Circuit has stated, '[o]ne of the purposes of adding 'offer to sell' to § 271(a) was to prevent exactly the type of activity [defendant] has engaged in, *i.e.*, generating interest in a potential infringing product to the commercial detriment of the rightful patentee.'"

-- ***C.R. Daniels, Inc. v. Naztec Intern. Group, LLC,*** No. ELH-11-01624, 2011 WL 6026293, at *12-13 (D. Md. Dec. 2, 2011) (internal citations; emphasis added) (quoting ***3D Systems, Inc. v. Aarotech Labs., Inc.,*** 160 F.3d 1373, 1379 (Fed. Cir. 1998)).

Case Law Does Not Require Pricing

"Although price terms were allegedly not discussed, Hanna's presentations were sales pitches, intended to generate customer interest and potential future sales . . . . [T]he audiences of Hanna's presentations were prospective customers . . . . Hanna's presentations were more than informational sessions lacking any commercial intent. Like *C.R. Daniels*, the presentations were designed to generate interest in the Eagle and produce future sales . . . . Sales of these sophisticated, technical products take significant time to progress to a final decision to purchase and presentations like Hanna's in Minnesota are part of the process. This squarely fits within the 'generating interest in a potential infringing product to the commercial detriment of the rightful patentee' definition that § 271(a)'s 'offer to sell' language was aimed at preventing."

-- ***Rudolph Techs., Inc. v. Camtek Ltd.,*** No. 15-1246 ADM/BRT, 2015 WL 5039295, at *9 (D. Minn. Aug. 26, 2015) (internal citations, quotations omitted; emphasis added)

Case Law Does Not Require Pricing

Compare limited holding of Defendants' case law citation:

" [T]ransmittal of e-mails containing technical data from SUMCO to Samsung Austin cannot constitute an 'offer to sale.' First, unlike the price quotation letters in *3D Systems*, the e-mails, while containing a description of the allegedly infringing wafers, do not contain any price terms. Accordingly, on their face, the e-mails cannot be construed as an 'offer' which Samsung Austin could make into a binding contract by simple acceptance."

-- ***MEMC Elec. Materials, Inc. v. Mitsubishi Materials Silicon Corp.,*** 420 F.3d 1369, 1376 (Fed. Cir. 2005) (emphasis added) (only evidence submitted of alleged offers were "emails containing technical data")

The Jury's Validity Verdict is Reasonable and Supported by Substantial Evidence

Presumption of Validity Alone is Substantial Evidence Supporting a Validity Verdict

"Under the law set by Congress, a jury or a court may reach a conclusion that a patent remains valid *solely* on the failure of the patent challenger's evidence to convincingly establish the contrary. A patent being presumed valid at birth, § 282, a patentee need submit *no* evidence in support of a conclusion of validity by a court or a jury."

-- ***Orthokinetics, Inc. v. Safety Travel Chairs, Inc.,*** 806 F.2d 1565, 1570 (Fed. Cir. 1986) (emphasis original)

Dr. Kuhn: Mizuno Does Not Disclose a Bulk Silicon Substrate (All Claims)

Q. What's the first claim that you analyze?

A. The first claim that I analyzed was the claim about the bulk silicon substrate, the SOI. And the Mizuno – whoops – Mizuno fails to disclose the bulk silicon substrate. And, of course, Professor Lee's invention is a bulk FinFET with a bulk substrate.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 129:16-22 (emphasis added)

Dr. Kuhn Clarified that Mizuno is SOI, Not Bulk

Q. (By Mr. Choung) Now, earlier, counsel showed you a picture -- a figure from Mizuno.
A. Yes, sir.
Q. Do you recall that figure?
A. 8B, maybe.
Q. And he asked you if there was a projection that was connected to a substrate?
A. Yes, sir?
Q. What kind of substrate was that?
A. That was actually an SOI device.
Q. All right. So that projection is not actually connected to a bulk substrate?
A. No, it's not.

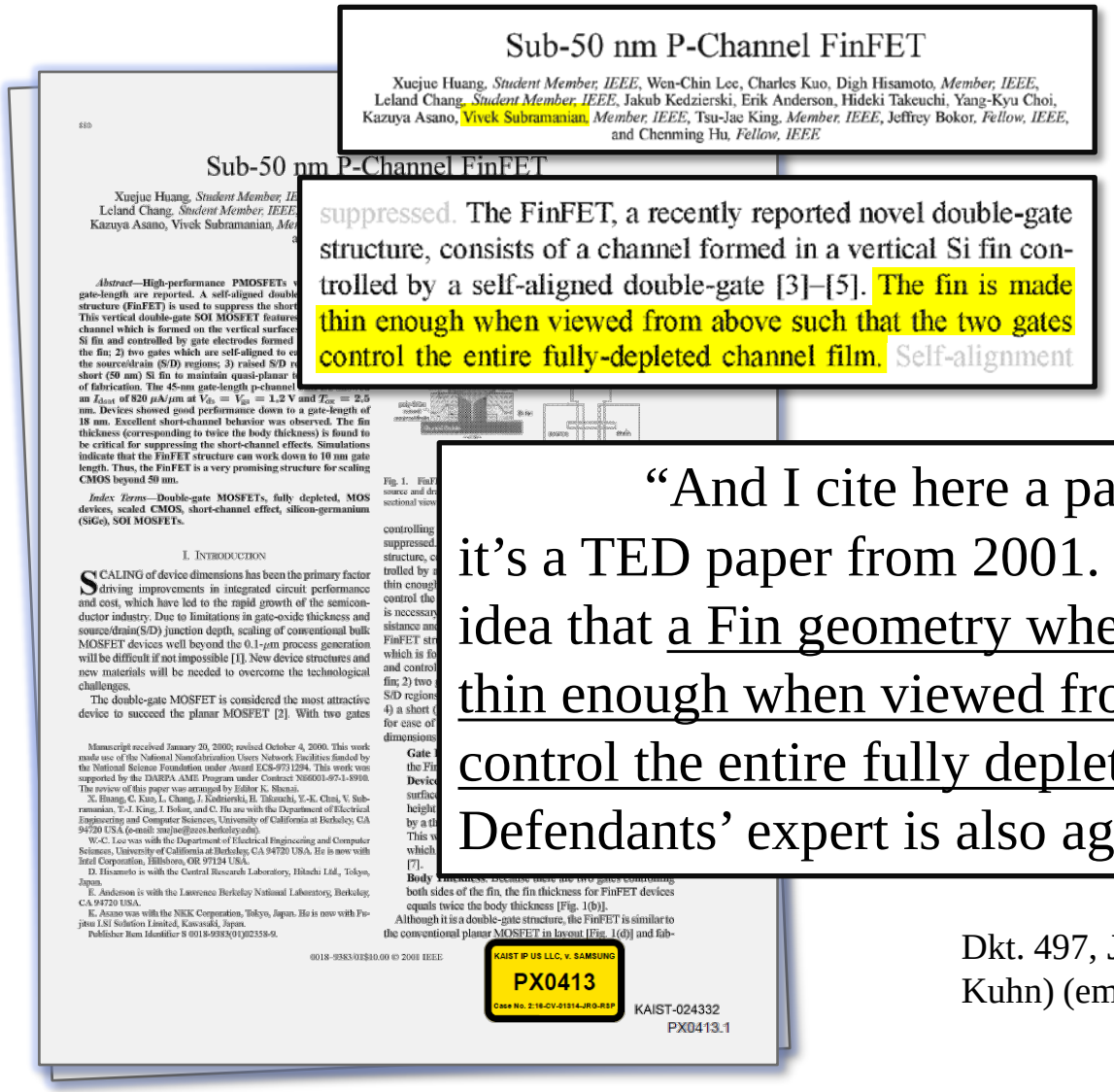
Dkt. 497, **June 14, 2018 PM Trial Tr.** at 195:8-18 (redirect; emphasis added)

Dr. Kuhn: Wall-Shape Creates Full Depletion

Q. All right. So what's the next part of the Claim 1 that you analyzed?
A. I analyzed the Fin active region, which is wall-shaped.
Q. So why is this significant?
A. This is this point of the wall-shaped Fin active region creating a full depleted region in the device. Keep in mind in the '055 Patent, the shape of the Fin active region, the wall-shape creates a fully depleted region, and that's important for producing the short channel effects.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 131:1-9 (emphasis added)

Dr. Kuhn: Dr. Subramanian's Paper Agreed that Fin Geometry Creates Full Depletion



Sub-50 nm P-Channel FinFET

Xuejue Huang, *Student Member, IEEE*, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, *Member, IEEE*, Leland Chang, *Student Member, IEEE*, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, *Member, IEEE*, Tsu-Jae King, *Member, IEEE*, Jeffrey Bokor, *Fellow, IEEE*, and Chenming Hu, *Fellow, IEEE*

suppressed. The FinFET, a recently reported novel double-gate structure, consists of a channel formed in a vertical Si fin controlled by a self-aligned double-gate [3]–[5]. The fin is made thin enough when viewed from above such that the two gates control the entire fully-depleted channel film. Self-alignment

KAIST IP US LLC, v. SAMSUNG
PX0413
Case No. 2:16-CV-01314-JRG-RSP

KAIST-024332
PX0413.1

"And I cite here a paper from Dr. Subramanian, it's a TED paper from 2001. And they also discuss this idea that a Fin geometry where you have a Fin that's made thin enough when viewed from above that the two gates control the entire fully depleted channel film. So the Defendants' expert is also agreeing with this observation."

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 131:24-132:5 (Dr. Kuhn) (emphasis added)

Dr. Kuhn: Mizuno Does Not Disclose a Wall-shape Fin (All Claims)

A. Mizuno is using this implant to control the short channel effects. <u>There's no evidence in Mizuno that they have any intention of using the Fin shape and gates to create the fully depleted Fin active region, the fully depleted Fin active region</u>. And there's an enormous amount of discussion about that implant and its relationship to other features in the device.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 132:8-14 (emphasis added)

Dr. Kuhn: Mizuno Does Not Disclose Non-Overlapping S/D and Gate Regions (All Claims)

Q. So is there anything in Mizuno that actually says or teaches this except where the said gate overlaps?

A. No, there's nothing that teaches that, and there's a fair number of things that teach opposite to that. If you'll notice the place where the Defendants have cited, it's formed with a source and drain region which are diffused layers. This is the same observation I made, except I'm recognizing that the diffusion will occur in all directions, which will put the source/drain under the gate. And there's no explicit disclosure as there is in the '055 patent that the -- the exception where the gate overlaps with the Fin active region. That's not mentioned in this.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 134:4-16 (emphasis added)

Dr. Subramanian Admitted No Express Disclosure of Non-Overlapping Regions in Mizuno

Q. Now, your evidence that the Mizuno reference describes a source and drain region that doesn't overlap with the gate region is the passage that you put at 9, 13 through 16, correct?

A. That's right.

Q. And that doesn't expressly say anything about overlap or lack or overlap, fair point?

A. That's true.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 14:22-15:4 (cross) (emphasis added)

Dr. Kuhn: Mizuno Does Not Disclose a Metal Layer (All Claims)

Q. So, Dr. Kuhn, does Mizuno ever specify – specifically expressly specify the use of a metal contact?

A. No, sir.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 135:14-22 (emphasis added)

Dr. Kuhn Addressed Mizuno's Al Wiring

"In a process with a metal contact, the usual material will be tungsten or a refractory material. So this aluminum wiring is not one of the source/drain with a gate. It's sitting up further. And that, in combination with the previous page which declares the use of polysilicon or amorphous silicon in the contact region, we have a pretty typical description of a DRAM architecture of this era.

So my assessment is Mizuno is simply discussing an architecture for their contact that was common at the time using a polysilicon in the contact region and then an aluminum wiring layer further up."

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 136:3-13 (emphasis added)

Dr. Kuhn: Mizuno Does Not Anticipate Claim 5

Dependent Claim 5 is not anticipated. Recall that Dependent Claim 5 is the claim about the parasitic capacitance between the gate and the bulk substrate. And it's the claim with the 20 nanometers to 800 nanometers. Mizuno does not teach this. So Dependent Claim 5 is not anticipated.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 137:20-24 (emphasis added)

Dr. Kuhn Explained that Mizuno Teaches a Different Parasitic Capacitance Than Claim 5

Q. Does Mizuno explicitly say anything about reducing parasitic capacitance?

A. Yes, it does. It does have a disclosure about parasitic capacitance, and that's Mizuno, Column 14, 41 through 48. And if you run through this disclosure, what they're talking about is what would be called in the art a junction capacitance. And that's a different capacitance than what we're talking about here.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 137:25-138:7 (emphasis added)

Dr. Kuhn: Mizuno Does Not Anticipate Claim 6

Q. And what about Claim 6, is there an independent reason why Claim 6 isn't anticipated?

A. Yes. Mizuno does not teach reducing the contact resistance by selecting the size of the contact to be greater than the width of the Fin or the length of the gate.

Q. Does Mizuno say anything about contact resistance?

A. No, it doesn't.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 138:11-17 (emphasis added)

Dr. Kuhn: Mizuno Fails to Anticipate Claim 13 for the Same Reasons It Fails to Anticipate Claim 1

Q. So does Mizuno fail to anticipate Claim 13 for the same reasons as Claim 1?

A. Yes, it does. All that common language, the bulk substrate, the Fin active region connected to the bulk substrate, the wall-shaped Fin active region, the source/drain overlap, and the metal layer, all those reasons are shared with Claim 1.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 140:15-21

Dr. Kuhn: Mizuno Also Fails to Disclose Claim 13's Unique "Wherein" Clause

Dr. Kuhn opined that Mizuno's Figure 17 did not depict enlarging within the oxidation layer approaching the substrate:

"You'll recall that the claim says enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk substrate. You'll notice here in the figure, it's straight. So that figure shows that this is not happening, and it's not disclosing it."

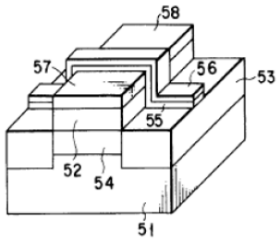
Dkt. 497, **June 14, 2018 PM Trial Tr.** at 140:15-21

Mizuno F

'055 Patent

13. A double-gate FinFET device, comprising:
a bulk silicon substrate;
a Fin active region which is a wall-shape single crystal silicon on a surface of the bulk silicon substrate connected to said bulk silicon substrate;
a second oxide layer which is formed up to a certain height of the Fin active region from the surface of silicon substrate;
a gate oxide layer which is formed on both side-walls of the Fin active region protruded from said second oxide layer;
a first oxide layer which is formed on the upper surface of said Fin active region with a thickness greater or equal to that of the gate oxide;
a gate which is formed on said first and second oxide layer;
a source/drain region which is formed on both sides of the Fin active region except where said gate overlaps with the Fin active region; and
a contact region and a metal layer which are formed at said source/drain and gate contact region,
wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidation layer as it approaches the bulk silicon substrate.

Figure 17 of Mizuno shows width remains CONSTANT:



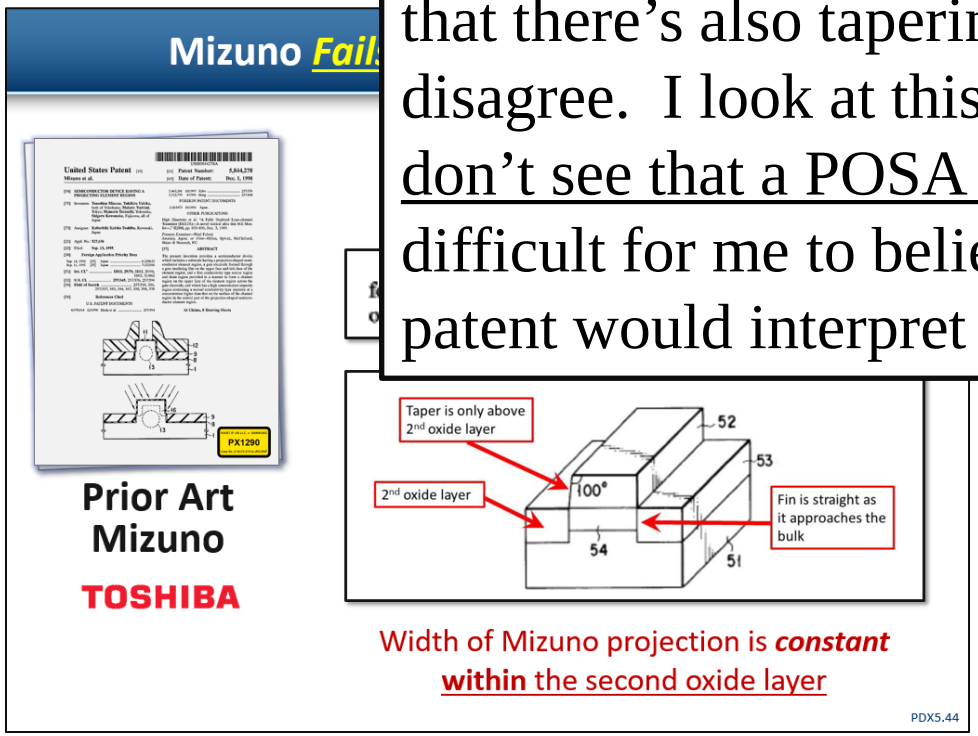
PDX5.43

Dr. Kuhn: Mizuno Also Fails to Disclose Claim 13's Unique "Wherein" Clause

Dr. Kuhn opined that Mizuno's Figure 18 did not depict enlarging within the oxidation layer approaching the substrate:

"Figure 18 clearly shows tapering on the top, and Dr. Subramanian has pointed out that he believes that there's also tapering on the bottom. And I just disagree. I look at this. I don't see tapering. I don't see that a POSA would see tapering. It's very difficult for me to believe that a person reading this patent would interpret that as tapered down here."

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 141:8-15 (emphasis added)



Dr. Kuhn: Mizuno Does Not Teach Contact Resistance (Claim 13)

A. Mizuno does not discuss reducing the resistance by enlarging. In fact, it never really discusses resistance at all.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 143:2-4

Dr. Kuhn: Mizuno Does Not Disclose Elements of Claims 11, 12, or 15 "At Any Level"

Q. Does Mizuno also fail to anticipate Dependent Claims 11 and 12?

A. Yes, it does. It never talks about – it never talks about doping junction depth at all. You'll recall that that's the claim that discusses where the junction depth is. <u>There's no mention of this in Mizuno at any level</u>, so neither of those two claims are anticipated.

Q. And what about Claim 15?

A. <u>Same thing</u>. Claim 15 does not – Mizuno does not disclose chamfering.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 139:12-21 (emphasis added)

Dr. Kuhn: No Motivation to Combine Mizuno and Seliskar

Q. So, Dr. Kuhn, would a person of ordinary skill in the art combine Mizuno and Seliskar?

A. No. First, they're incompatible designs. This is a really different device than we're talking about with Mizuno. One of them is SOI. One of them is not. One of them is 3D. One of them is planar. And they're both a long way from the '055 in nodes, Mizuno being five nodes away, Seliskar being 10 nodes away. But they're still five nodes from each other.

The reason this is important is because five nodes is five cycles of processes and manufacturing tools. It is not easy to jump even from one node to the other. Jumping five nodes is extremely hard. Jumping 10 is just silly.

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 149:23-150:10 (emphasis added)

Dr. Kuhn: No Motivation to Combine Mizuno and Hieda

Dr. Kuhn identified two de-motivating differences between Mizuno and Hieda, the first being implant versus no implant:

"Now there's two significant difference [*sic*] between the two patents. Keep – recall that from Mizuno, we have this architecture with this hovering implant, and a lot of discussion about how to create short channel effects by operating against that implant. There's no discussion of any movement of the Fin active region for this.

Hieda has no implant in the middle. There source/drain regions are highlighted here just as visual aid, but notice there's nothing in there that's equivalent to this hovering implant."

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 155:2-19 (emphasis added)

Dr. Kuhn: No Motivation to Combine Mizuno and Hieda

Dr. Kuhn identified a second de-motivating difference between Mizuno and Hieda—their respective S/D doping strategies:

"They're quite different. Recall, Mizuno has a doping strategy that we've discussed before with regards to the source/drain intruding under the gate. It's a layer that does not fill the entire region of the projection. It's just working around the edge of the projection as you see here.

In Hieda, one of the key features of Hieda is the source/drain region that intrudes under the gate. But the source/drain region also fills the entire projection. So they're really dramatically different architectures. And a POSA would not either grab this architecture and put it over there, nor would they start trying to stand this architecture just because they saw this patent because of all the interaction with the central doping region."

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 155:2-19 (emphasis added)

Dr. Kuhn Responded to "Breakdown" Argument

"Okay. What the Defendants are pointing to is the idea of the chamfering of the slide. And they're point to the idea that there will be areas here in the corner with breakdown.

And the Defendants have discussed the breakdown features, and those are important features in our technology generations.

The issue here is that with this implant region, as I showed you the source/drain region design that Mizuno is using, we have a situation where a POSA would not be motivated to start chomping away at this . . . . [I]t's just a situation where a POSA would not be willing to risk the architecture that's so characteristic of this patent in order to achieve a gain that they might be able to achieve by some other technique."

Dkt. 497, **June 14, 2018 PM Trial Tr.** at 155:2-19 (emphasis added)